ABSTRACT OF THE DISCLOSURE

An apparatus includes a field-programmable gate array (FPGA). The FPGA includes a first FPGA tile, and the first FPGA tile includes a plurality of functional groups (FGs), a regular routing structure, and a plurality of interface groups (IGs). The plurality of FGs are arranged in rows and columns with each of the FGs being configured to receive regular input signals, perform a logic operation, and generate regular output signals. The regular routing structure is coupled to the FGs and configured to receive the regular output signals, route signals within the first FPGA tile, and provide the regular input signals to the FGs. The plurality of IGs surround the plurality of FGs such that one IG is positioned at each end of each row and column. Each of the IGs is coupled to the regular routing structure and configured to transfer signals from the regular routing structure to outside of the first FPGA tile.